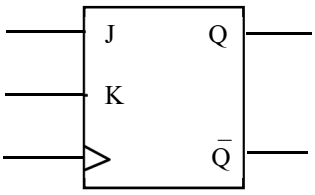
Tutorial 6 Questions

Please try out these self-study questions (labeled "SS"). These will not be discussed in class and solutions will be provided later.

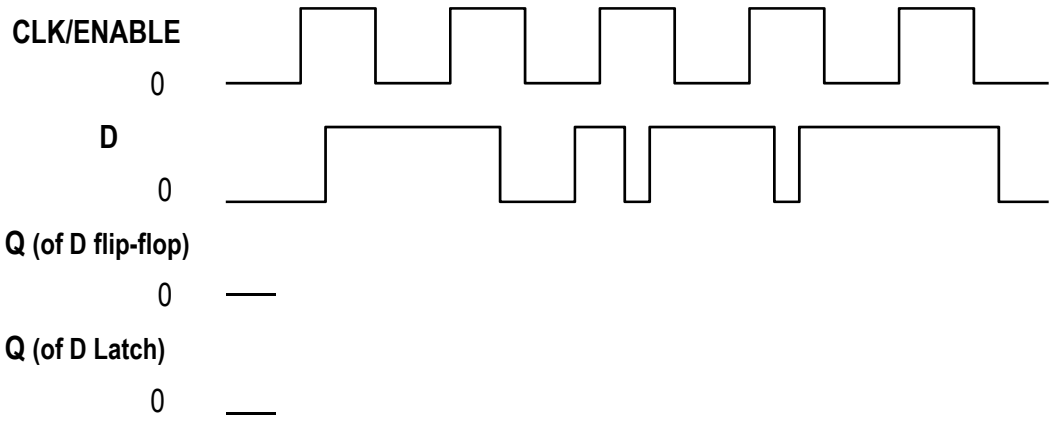
Flip Flops



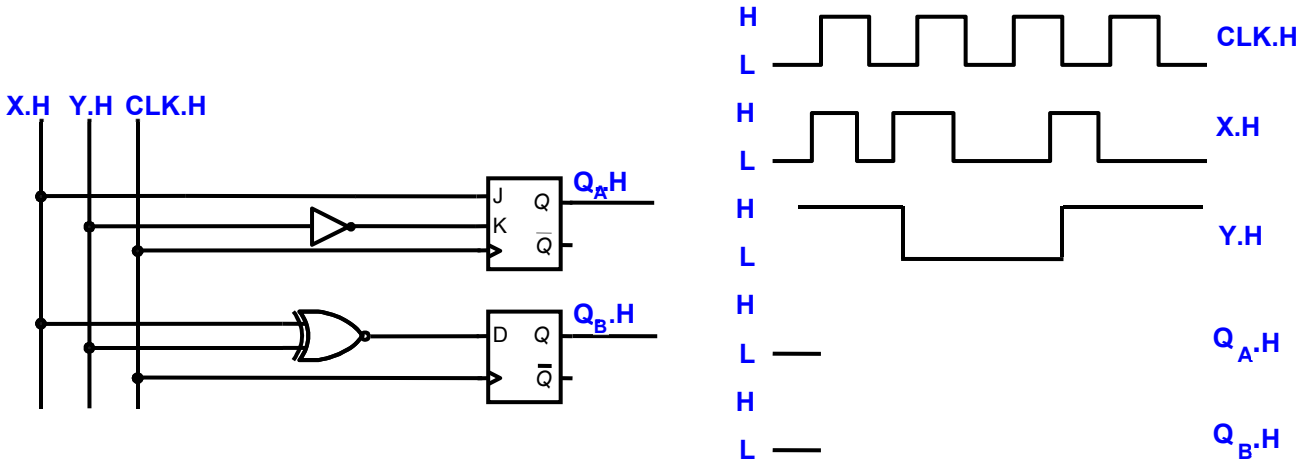
SS1. Using additional logic gates, show how a JK flip-flop be modified to operate as a D flip-flop.

SS2. Write a Verilog program to describe a JK flip-flop and check your solution using the Xilinx tools. (Refer to the characteristic table of the JK flip-flop for some help!)

Q1. The D and CLK/ENABLE input waveforms shown below are applied to a negative-edge triggered D flip-flop & a D Latch. Clearly draw the output Q waveforms of the devices and neglect all propagation delays.

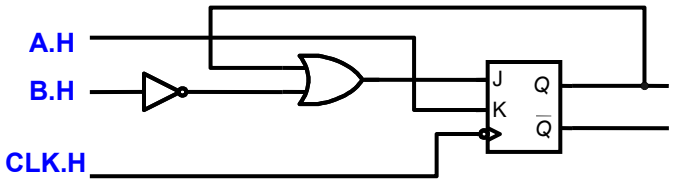


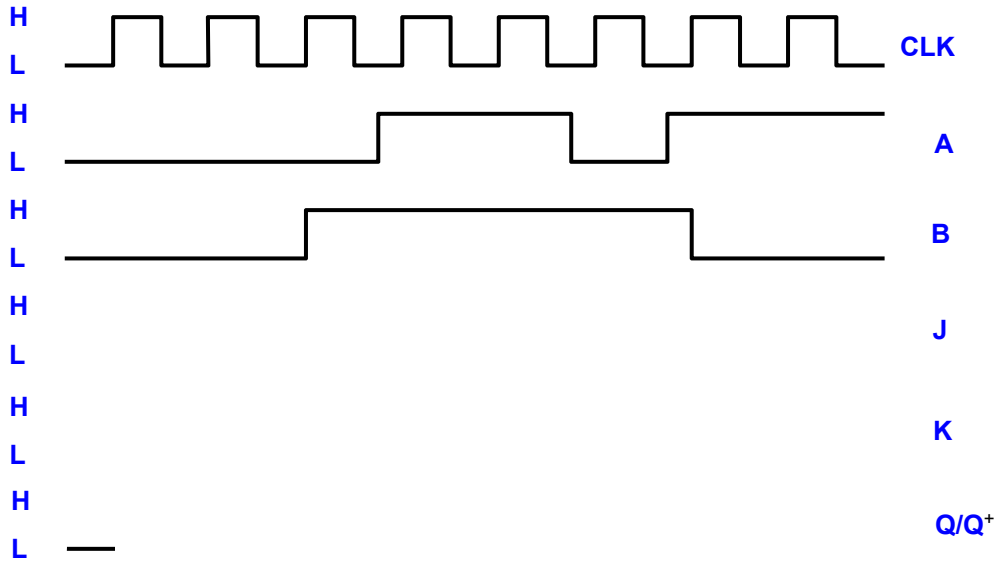
Q2. Given the circuit diagram below, complete the timing diagram below by filling in Q_A and Q_B. Include the propagation delays tp_{HL} and tp_{LH}.



Q3. (a) Given the circuit diagram below, complete the timing diagram below by filling in J, K and Q. Neglect all propagation delays in this question.

(b) The circuit below represents a type of AB flip flop, fill in its characteristic table and condensed characteristic table below.





A	B	Q	Q^+

Characteristic Table

A	B	Q^+

Condensed Characteristic Table